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APPARATUS FOR AND METHOD OF IMPLEMENTING TIME-INTERLEAVED ARCHITECTURE

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APPARATUS FOR AND METHOD OF IMPLEMENTING TIME-INTERLEAVED ARCHITECTURE

BACKGROUND

Time interleaved (or multi-channel) architecture is commonly used in semiconductor or other devices to provide parallelism in circuit design. As circuit speed, resolution and complexity are ever increasing, the demands on circuit design are immense. Time interleaved architecture assists in meeting these demands by providing a mechanism for relaxing the criteria without foregoing circuit performance. As shown in Fig. 8(a), for example, the time-interleaved architecture is typically composed of a plurality of parallel channel devices 82a, 82b, . . . 82m generating a plurality of channel output signals which are ultimately combined as a single output using a device such as multiplexer 84.

Many advantages arise from the use of such a time-interleaved architecture. For example, in a circuit design requiring a final speed of *Fs*, utilizing a time-interleaved architecture, a series of *m* channels (e.g., channels 1, 2, . . . m, as in Fig. 8(a)) can be used. Where each channel is designed to perform the required functions in parallel, the individual channels need only be designed to perform at the less demanding speed of *Fs/m*. The circuit design on each individual channel therefore is relaxed and more manageable.

To successfully implement any time-interleaved architecture, a precise delay multi-phase clock generator is required. As shown in Fig. 8(a), a plurality of sample and hold devices 80a, 80b, . . . 80m must sample the input signals at precise intervals to provide the correct input signal samples to the plurality of channel devices 82a, 82b, . . .

82m. The multi-phase clock signals $\Phi 1$, $\Phi 2$, . . . Φm must therefore be precise in the time intervals between clock phases. Ideally, the delay between any adjacent phases should be exactly the same, i.e., $\Phi 1$, $\Phi 2$, . . . Φm uniformly distributed within one clock period m/Fs, $\Delta td_1 = \Delta td2 = \ldots = \Delta td_m = 1/Fs$, as shown in Fig. 8(b).

In real-world applications, however, random variations of the sampling signals is unavoidable. The instability of every individual clock phase itself makes precise sampling difficult. The instability is often caused by noise sources (commonly known as "jitter") on the device itself (e.g., integrated circuit or "chip"). Jitter raises the noise floor, thus, reducing signal-to-noise ratio (SNR). Variations in the sampling signals may also be attributed to mismatches in the device, the channel, or both. Such mismatches may introduce tones into the operation, thereby reducing spurious-free dynamic range (SFDR). Such random variations in the sampling signals is often critical to the effectiveness of the time-interleaved architecture.

SUMMARY

In accordance with a preferred embodiment, a time-interleaved (or multi-phase) architecture is provided having individual control of a plurality of output signals or phases. The time-interleaved architecture may be implemented using a first set of delay cells such as those in a ring oscillator or a delay line device receiving overall control of its output signals by a global control signal. The global control signal may be issued by a phase-locked loop, delay-locked loop, or other like structure. A second set of delay cells is provided to further delay the output signals produced by the first set of delay cells. The second set of delay cells are controlled by individual control signals

uniquely calibrated in accordance with a preferred embodiment of the invention to provide uniform (or substantially) uniform time spacing between output signals.

BRIEF DESCRIPTION OF THE DRAWINGS

Many advantages, features, and applications of the invention will be apparent from the following detailed description of preferred embodiments of the invention, which is provided in connection with the accompanying drawings, in which:

Fig. 1 is a block diagram illustrating a time-interleaved architecture implemented with a ring oscillator in accordance with a preferred embodiment of the invention;

Fig. 2 is a block diagram illustrating a time-interleaved architecture implemented with a delay line in accordance with a preferred embodiment of the invention;

Fig. 3 is a block diagram illustrating a time-interleaved architecture implemented with a phase-locked loop (PLL) in accordance with a preferred embodiment of the invention;

Fig. 4 is a block diagram illustrating a time-interleaved architecture implemented with a delay-locked loop (DLL) in accordance with a preferred embodiment of the invention;

Fig. 5 is a timing diagram illustrating a calibration method in accordance with a preferred embodiment of the invention;

Fig. 6 is a block diagram illustrating calibration loops in accordance with a preferred embodiment of the invention;

Fig. 7 is a timing diagram for a delay line architecture addressed in accordance with a preferred embodiment of the invention;

Fig. 8(a) is a block diagram illustrating a known time-interleaved architecture; and

Fig. 8(b) is the ideal timing diagram for the known time-interleaved architecture illustrated in Fig. 8(a).

DETAILED DESCRIPTION

Preferred embodiments in application of the invention will now be described with reference to Figures 1-7. Other embodiments may be realized and structural or logical changes may be made to the disclosed embodiments without departing from the spirit or scope of the invention. Although the embodiments are particularly described as applied to a time-interleaved (or multi-channel) architecture in the form of a multi-phase clock, it should be readily apparent that the invention may be embodied in any device or system having the same or similar problems.

In accordance with a preferred embodiment of the invention, a first set of delay cells 12a, 12b, . . . 12n are provided to produce a series of output signals, as shown in Figure 1. In this illustrated embodiment, the first set of delay cells 12a, 12b, . . . 12n are presented in a series or cascade format and embodied in a ring oscillator 10,

which is part of a time-interleaved architecture such as a multi-phase clock generator. Other configurations, implementations and applications of the invention, however, should be readily apparent to those skilled in the art. A global control signal (control voltage Vctrl) is commonly connected to the control inputs of each of the first set of delay cells 12a, 12b, . . . 12n in a manner well known in the art. Typically, such a global control signal is output from a feedback control loop (e.g., phase-locked loop (PLL), or other equivalent circuit) (not shown in Fig. 1) so as to control the general timing of output signals produced by delay cells 12a, 12b, . . . 12n in a manner well known in the art.

As illustrated, the output signals produced by delay cells 12a, 12b, . . . 12n are received by a second set of delay cells 14a, 14b, . . . 14n, 15a, 15b, . . .15n. The second set of delay cells may take any known form, and are typically the same structures used in the first set of delay cells 12a, 12b, . . . 12n. Like the first set of delay cells, the second set of delay cells 14a, 14b, . . . 14n, 15a, 15b, . . .15n generate delayed output signals in response to the signals received at their inputs. Unlike the first set of delay cells, however, the second set of delay cells do not utilize a global control signal to control the timing of their delayed outputs. Instead, the second set of delay cells 14a, 14b, . . . 14n, 15a, 15b, . . .15n receive as inputs a series of individual control signals Vctrl1, Vctrli, . . . Vctrlj, Vctrlk, Vctrl*l*, . . . Vctrlm that provide the ability to individually control each delay cell 14a, 14b, . . . 14n, 15a, 15b, . . .15n independently of the other. The individual control signals preferably provide a mechanism for compensating for any delay mismatch in the time-interleaved architecture so as to provide uniform (or at least substantially uniform) time intervals between output

phases, as well as providing a mechanism for individually controlling the output phases for any purpose desired, including non-identical pulse widths or other individual output phase control.

In the illustrated embodiment, the series of individual control signals adjust the time intervals of (or time spacing between) respective output signals issued by ring oscillator 10 without affecting any global loop control provided by global control signal Vctrl. Indeed, in this illustrated embodiment, one channel 18a of the time-interleaved architecture is directly aligned with global control signal Vctrl by tapping the global control signal Vctrl as the input control signal for its second series delay cell 14a, as shown in Fig. 1.

For the illustrated embodiment, a channel output signal $\phi 1$, ϕi, . . . ϕj, ϕk, ϕl, . . . ϕm is provided for each channel (e.g., only one channel 18a is specifically illustrated) by a respective output buffer 16a, 16b, . . .16n, 17a, 17b, . . . 17n. Output buffers may be useful in a variety of applications such as, for example, where the output signal is a clock phase needed to drive internal circuitry of an (on-chip) integrated electronic system.

Fig. 2 illustrates a preferred embodiment of the invention employing a first set of delay cells 22a, 22b, . . . 22n in the form of delay line 20. The structure (and operation) of this embodiment is substantially similar to that described above with respect to Fig. 1. A second set of delay cells 24a, 24b, . . . 24n, 25a, 25b, . . . 25n receive output signals produced by the first set of delay cells 22a, 22b, . . . 22n to, in

turn, produce delayed output signals to be relayed to output buffers 26a, 26b, . . . 26n, 27a, 27b, . . . 27n. A series of individual control signals Vctrl1, Vctrli, . . . Vctrlj, Vctrlk, Vctrll, . . . Vctrlm is provided for the individual control of delay cells 24a, 24b, . . . 24n, 25a, 25b, . . . 25n, respectively. This series of individual control signals uniquely offers fine adjustment control for each one of the second set of delay cells in addition to the overall control provided by global control signal Vctrl.

Preferably, at least one individual control signal (e.g., Vctrl1) is aligned with global control signal Vctrl, as shown in Fig. 2. Unlike the initial delay cell 12a in the first set of delay cells 12a, 12b, . . . 12n making up the ring oscillator 10 in Fig. 1, the initial delay cell 22a of the second set of delay cells 22a, 22b, . . . 22n making up delay line 20 in Fig. 2 does not receive as its input a feedback signal from a downstream delay cell. Instead, the initial delay cell 22a receives as its input an external reference clock signal in this illustrated embodiment. Channel output signals $\phi 1$, ϕi, . . . ϕj, ϕk, ϕl, . . . ϕm are provided for each channel (e.g., only one channel 28a is specifically illustrated) by respective output buffers 26a, 26b, . . . 26n, 27a, 27b, . . . 27n.

The time-interleaved architectures depicted in Figs. 1 and 2 can easily be applied to a variety of applications. A phase-locked loop (PLL)-based multi-phase clock generator system may be formed, for example, with the addition of loop filter 30, charge pump 32, and phase detector 34, as shown in Fig. 3. Phase detector 34 receives both an external reference clock signal and one (e.g., $\phi 1$) of the plurality of channel output signals $\phi 1$, $\phi 2$, $\phi 3$, $\phi 4$, $\phi 5$, $\phi 6$, $\phi 7$, $\phi 8$ provided by a respective one (e.g., 16a) of the plurality of output buffers 16a, 16b, 16c, 16d, 17a, 17b, 17c, 17d. Phase

detector 34 outputs a directional control signal based on a comparison of output phases of the reference clock signal and one (e.g., $\phi 1$) of the channel output signals so as to align the channel output signal with the reference clock signal. Charge pump 32 converts the directional control signal generated by phase detector 34 into an output current. Loop filter 30 provides a filtered main output control voltage in the form of global control signal Vctrl, which corresponds to the output current provided by charge pump 32.

The global control signal Vctrl is input to each of the first set of delay cells 12a, 12b, 12c, 12d to provide overall control of the delay cells. Output signals from the first set of delay cells are input to a second set of delay cells 14a, 14b, 14c, 14d, 15a, 15b, 15c, 15d. The second set of delay cells produces delayed output signals based on individual control signals Vctrl1, Vctrl2, Vctrl3, Vctrl4, Vctrl5, Vctrl6, Vctrl7, Vctrl8 input to the second set of delay cells. Because individual control signal Vctrl1 is tied to the output (Vctrl) of loop filter 30, individual control signal Vctrl1 can be made to be aligned with the external reference clock. Delayed output signals from the second set of delay cells 14a, 14b, 14c, 14d, 15a, 15b, 15c, 15d are provided to output buffers 16a, 16b, 16c, 16d, 17a, 17b, 17c, 17d, which, in turn, generate the plurality of channel output signals $\phi 1$, $\phi 2$, $\phi 3$, $\phi 4$, $\phi 5$, $\phi 6$, $\phi 7$, $\phi 8$.

A similar implementation of the time-interleaved architecture of Fig. 2 is made by adding loop filter 40, charge pump 42, and phase detector 44 to form a delay-locked loop (DLL)-based multi-phase clock generator system, as shown in Fig. 4. As with the system of Fig. 3, phase detector 44, charge pump 42, and loop filter 40 in this

exemplary system cooperate to produce global control signal Vctrl based on a comparison of an external reference clock and one of the channel output signals $\phi 1$, $\phi 2$, $\phi 3$, $\phi 4$, $\phi 5$, $\phi 6$, $\phi 7$, $\phi 8$ generated by output buffers 26a, 26b, 26c, 26d, 27a, 27b, 27c, 27d. The use of first set of delay cells 22a, 22b, 22c, 22d and second set of delay cells 24a, 24b, 24c, 24d, 25a, 25b, 25c, 25d in conjunction with individual control signals Vctrl1, Vctrl2, Vctrl3, Vctrl4, Vctrl5, Vctrl6, Vctrl7, Vctrl8 produces a series of delayed output signals for use in generating channel output signals $\phi 1$, $\phi 2$, $\phi 3$, $\phi 4$, $\phi 5$, $\phi 6$, $\phi 7$, $\phi 8$ by output buffers 26a, 26b, 26c, 26d, 27a, 27b, 27c, 27d, in the manner described in detail above.

As should be readily apparent, a number of different mechanisms can be employed to generate the individual control signals Vctrl1, Vctrli, . . . Vctrlj, Vctrlk, Vctrl, . . . Vctrlm used in the time-interleaved architectures described herein. In accordance with a preferred embodiment of the invention, calibration loops are provided to produce the individual control signals, as will be described in detail below in connection with an exemplary 8 channel ($\phi 1$, $\phi 2$, $\phi 3$, $\phi 4$, $\phi 5$, $\phi 6$, $\phi 7$, $\phi 8$) architecture. In the calibration loops, one phase (e.g., $\phi 1$) is aligned to the external reference clock used to provide global feedback control (e.g., using PLL, DLL, etc.) of the time-interleaved architecture. Accordingly, one of the individual control signals (e.g., Vctrl1) can be taken as the same control signal (e.g., Vctrl) generated by the global feedback loop. The remaining individual control signals Vctrl2, Vctrl3, Vctrl4, Vctrl5, Vctrl6, Vctrl7, Vctrl8 are generated in a bi-sected manner, in accordance with this exemplary embodiment described in detail below.

As shown in Fig. 5, the different channel output phases $\phi 1$, $\phi 2$, $\phi 3$, $\phi 4$, $\phi 5$, $\phi 6$, $\phi 7$, $\phi 8$ are spaced in time relative to each other, as represented by time intervals Δtd_{x-y} (representing the time between phase ϕx and ϕy). By comparing the individual time intervals Δtd_{x-y} between phases (or channel outputs) $\phi 1$, $\phi 2$, $\phi 3$, $\phi 4$, $\phi 5$, $\phi 6$, $\phi 7$, $\phi 8$ the appropriate individual control signals Vctrl2, Vctrl3, Vctrl4, Vctrl5, Vctrl6, Vctrl7, Vctrl8 can be generated. For illustration purposes, the different individual control signals can be divided into different reference levels as they relate to their respective controlled channel outputs (or phases):

Reference level 5: $\phi 1$ $\phi 2$ $\phi 3$ $\phi 4$ $\phi 5$ $\phi 6$ $\phi 7$ $\phi 8$

Reference level 4: $\phi 1$ $\phi 3$ $\phi 5$ $\phi 7$

Reference level 3: $\phi 1$ $\phi 5$

Reference level 2: $\phi 1$

Reference level 1: external reference clock

For example, the first reference level is taken as the external reference clock signal. Once $\phi 1$ is in lock with the reference clock, phase $\phi 1$ operates as the second level of reference. For the third reference level, to generate individual control signal Vctrl5 associated with adjustment of phase $\phi 5$, a comparison is made of the time interval (Δtd_{1-5}) between $\phi 1$ and $\phi 5$ and the time interval (Δtd_{5-1+}) between $\phi 5$ and the subsequent $\phi 1$ (represented by "$\phi 1+$" in Fig. 5). For the fourth reference level, to generate individual control signal Vctrl3 associated with adjustment of phase $\phi 3$, a comparison is made of the time interval (Δtd_{1-3}) between $\phi 1$ and $\phi 3$ and the time

interval (Δtd_{3-5}) between $\phi 3$ and $\phi 5$. Also, as part of the fourth reference level, a comparison is made of the time interval (Δtd_{5-7}) between $\phi 3$ and $\phi 5$ and the time interval (Δtd_{7-1+}) between $\phi 7$ and subsequent phase $\phi 1$ to generate Vctrl7. The remaining individual control signals can be generated in like fashion for the fifth reference level: comparing Δtd_{1-2} and Δtd_{2-3} to generate Vctrl2; comparing Δtd_{3-4} and Δtd_{4-5} to generate Vctrl4; comparing Δtd_{5-6} and Δtd_{6-7} to generate Vctrl6; and comparing Δtd_{7-8} and Δtd_{8-1+} to generate Vctrl8.

Utilizing these calibration loops, stability can be achieved at each level, without affecting the results of a previous level, with each calibration loop in lock. Preferably, these calibration loops are performed simultaneously using a variety of known mechanisms for performing the functionality described above. A series of delay comparators and charge pumps can be used, for example, to generate the individual control signals Vctrl*x*. As shown in Fig. 6, delay comparator 60a compares phases $\phi 1$, $\phi 5$, and $\phi 1+$, and accordingly, generates a comparison signal(s) for input to charge pump 60b. Charge pump 60b converts the comparison signal(s) into a form used in the time-interleaved architecture as individual voltage control signal Vctrl5. Similarly, delay comparators 61a, 62a, 63a, 64a, 65a, 66a and charge pumps 61b, 62b, 63b, 64b, 65b, 66b are used to generate individual voltage control signals Vctrl3, Vctrl7, Vctrl2, Vctrl4, Vctrl6, and Vctrl8, respectively. To generate these individual control signals, comparison is made of phases $\phi 1$, $\phi 3$, $\phi 5$ by delay comparator 61a; $\phi 5$, $\phi 7$, $\phi 1+$ by delay comparator 62a; $\phi 1$, $\phi 2$, $\phi 3$ by delay comparator 63a; $\phi 3$, $\phi 4$, $\phi 5$ by delay comparator 64a; $\phi 5$, $\phi 6$, $\phi 7$ by delay comparator 65a; and $\phi 7$, $\phi 8$, $\phi 1+$ by delay comparator 66a, as shown in Fig. 6.

In accordance with a preferred embodiment, delay line 20 used in the DLL-based multi-phase clock generator system illustrated in Fig. 4 includes delay cells 22b, 22c, 22d that receive as their inputs channel output signals $\phi 2$, $\phi 3$, $\phi 4$, $\phi 6$, $\phi 7$, $\phi 8$ directly from output buffers 26a, 26b, 26c, 27a, 27b, 27c. The multi-phase clock generator system shown in Fig. 4 can be used without this modification, i.e., with the delay cells 22b, 22c, 22d receiving delayed signals from previous delay cells, but will likely experience a delay offset in the distribution of phases $\phi 1$, $\phi 2$, $\phi 3$, $\phi 4$, $\phi 6$, $\phi 7$, $\phi 8$, as demonstrated in Fig. 7.

While preferred embodiments of the invention have been described and illustrated, it should be apparent that many modifications (e.g., structural, logical, etc.) to the embodiments and implementations of the invention can be made without departing from the spirit or scope of the invention. For example, while the exemplary embodiments disclosed herein depict the use of output buffers (e.g., output buffers 16a, 16b, . . . 16n, Fig. 1), the invention can easily be implemented without the use of output buffers. The invention may be embodied in time-interleaved (or other) architecture both on a single device (e.g., integrated circuit), or in conjunction with one or more additional devices, for real-time or non-real-time operation.

The embodiments illustrated above referred to the use of the same (or substantially the same) delay cells (e.g., 12a, 12b, . . . 12n, 14a, 14b, . . . 14n, 15a, 15b, . . . 15n) shown in Fig. 1, for example. It is likely, however, that any number or combination of different delay cells can be used in implementing the invention. Although the second set of delay cells (e.g., 14a, 14b, . . . 14n, 15a, 15b, . . . 15n)

depicted in the exemplary embodiments described herein associate two second set delay cells (e.g., 14a, 15a) to every one first set delay cell (e.g., 12a), it should be apparent that any number (e.g., 0, 1, 2, 3, . . .N) of second set delay cells may be associated with each one of the first set of delay cells (e.g., 12a, 12b, . . . 12n).

The references to signaling parameters such as voltage control signals Vctrl, Vctrl1, . . . Vctrlm, etc. (Fig. 1) or output current from charge pump 32 are for illustrative purposes only. Any known signaling parameters may be utilized in implementing the invention. While the series of individual control signals Vctrl1, Vctrli, . . . Vctrlj, Vctrlk, Vctrl, . . . Vctrlm are shown as useful in fine adjustment control in addition to a global control signal used by a device such as ring oscillator 10, it should be apparent that the series of individual control signals may also be used in lieu of the global control signal.

As used herein, the term "uniform time spacing" refers to the spacing between output signals themselves, as well as the spacing between transitions of one or another signal, or any other portion of the output signals. In practice, the output pulses may have different shapes due to device imperfections, etc. Thus, the uniform time spacing between output signals may best be achieved for the transitions of such signals. The term further includes the implementation of "substantially" uniform time spacing, which includes signals that may deviate slightly from the uniform spacing applied. Moreover, it should be understood that the term "uniform" time spacing may refer to identical time-wise spacing of output signals, as well as any other standard or set relationship between individual output signals. Some implementations of other

"uniform" spacing may include, for example, specific relationships between one or all successive output signals (e.g., one time period being set at a rational fraction such as 3/5 or 8/7 of another time period, one time period being the sum/difference of several other time periods, etc.).

The modules described herein, particularly those illustrated in (or inherent from) Figs. 1-7, may be one or more components in various combinations. Although the modules are shown or described as physically separated components (e.g., delay comparator 60a, charge pump 60b, Fig. 6), it should be readily apparent that individual modules may be omitted, combined, or further separated into a variety of different components, sharing different elements as required for the particular implementation of the embodiments disclosed herein. Accordingly, the invention is not limited by the description or drawings of this disclosure, but only by the appended claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is: